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(71) Applicant: **XEROX CORPORATION**
Rochester New York 14644 (US)

(72) Inventors:
- **Yao, William**
  Los Altos, California 94024 (US)
- **Fulks, Ronald T.**
  Mountain View, California 94049 (US)
- **Ho, Jackson**
  Palo Alto, California 94301 (US)

(74) Representative: **Johnson, Reginald George et al**
Rank Xerox Ltd
Patent Department
Parkway
Marlow Buckinghamshire SL7 1YL (GB)

(54) An integrated dark matrix for an active matrix liquid crystal display and manufacturing method

(57) The invention provides an integrated dark matrix for an active matrix liquid crystal display. A plurality of pixel electrodes (38,72) overlap (710) at least one of a plurality of gate lines (34) and a plurality of data lines (32). A perimeter of the pixel electrodes overlaps the gate lines and/or data lines by twice the distance (718) that the pixel electrode is above the gate and data lines, respectively to obtain a viewing angle of over 60 degrees.

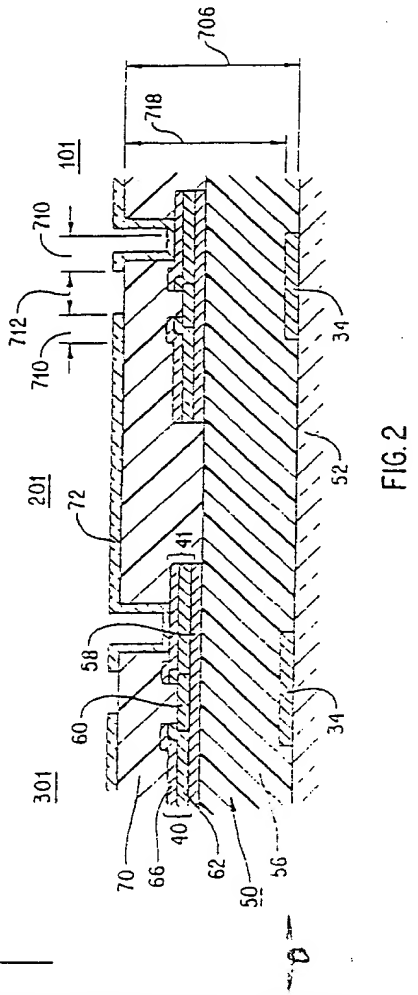

FIG. 2

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Description

The invention generally relates to an active matrix liquid crystal display device overlapping pixel electrodes with gate lines and data lines to achieve an integrated dark matrix using a five mask display architecture.

Active matrix liquid crystal displays (AMLCD) improve display quality by using thin film transistors (TFT) to drive pixel electrodes. The AMLCD is used in display portions of many high volume products such as laptops. Thus, there is great interest to improve manufacturing yields by simplifying the manufacturing processes leading to increased product reliability and reduction in product cost.

The pixel electrode in AMLCD designs usually comprises a layer of indium-tin-oxide (ITO) because the ITO is both transparent and conductive. Current AMLCD designs form a passivation layer over the ITO layer. A liquid crystal material is then placed over the passivation layer and a common electrode is formed over the liquid crystal material completing the AMLCD device. Conventionally, the AMLCD is formed on a surface of a transparent substrate. The pixels of the AMLCD are formed by parallel gate lines and parallel data lines. The gate lines and data lines are perpendicular to each other forming a matrix of pixel regions on the surface of the substrate. A pixel electrode is formed in each pixel region and connected to a TFT.

Depending on the polarization of the liquid crystal material, a pixel is in either a normally clear state or a normally opaque state. The state of the liquid crystal mateial is controlled by the voltage potential between the common electrode and the pixel electrode. When the pixel electrode is activated, the liquid crystal material changes state either from the clear state to opaque state or vice versa.

Since the pixel electrodes are conductive and formed on the same surface level as the data lines, the pixel electrodes must be prevented from contacting the data lines, thus leaving gaps between the data liness and the pixel electrodes. For a normally clear liquid crystal material, when a pixel electrode is activated, light passes through the gaps degrading the display quality. For a normally opaque liquid crystal material, the liquid crystal material above the gap between the pixel electrodes and data lines remain always opaque regardless of the activation of the pixel electrode. However, since the data lines are shared among many pixels, the voltage potential on these signal lines change the state of the liquid crystal material above them from opaque to clear and light escapes from the gaps through these clear portions. Thus, light undesirably escapes through the gaps independent of whether the liquid crystal material is normally clear or normally opaque.

Accordingly, conventional AMLCD devices form a dark matrix on the common electrode to block the light that escapes through the gaps between the pixel electrodes and the data lines. Usually, the dark matrix overlaps the gaps by about 5 microns to achieve acceptable display quality.

Since AMLCDs are commonly used in portable devices which have limited battery lifetimes, a new AMLCD structure is designed to reduce power consumption of the AMLCD. This structure is described in detail in the parent case EP-A-0 679 922. The new structure places the ITO layer above the passivation layer so that the voltage necessary to drive the pixel electrode is reduced thus reducing the power consumption of the AMLCD.

Placing the ITO layer above the passivation layer increases the gap through which light can escape. The vertical distance separating the pixel electrode and the data line is increased by the thickness of the passivation layer. To maintain display quality, the dark matrix area on the common electrode must be increased. However, increasing the dark matrix area reduces the effective pixel region which also causes degradation in display quality.

One object of this invention is to provide a dark matrix by forming a plurality of gate lines over a substrate, a plurality of data lines over the substrate and a plurality of pixel electrodes over the gate and data lines so that a perimeter of each pixel electrode overlaps at least one of a portion of the gate lines and a portion of the data lines.

The pixel electrode is formed above the gate lines by a first distance and above the data lines by a second distance. The pixel electrode overlaps the gate lines by at least twice the first distance and overlaps the data lines by at least twice the second distance to obtain a viewing angle of greater than 60 degrees.

Another object of the invention is to provide a method for manufacturing a dark matrix by overlapping the pixel electrode over gate and data lines.

Accordingly, the present invention provides an active matrix liquid crystal display device and method for manufacturing same as claimed in the appended claims.

The invention will be described further, by way of example, with reference to the accompanying drawings, wherein:

Fig. 1 is a top plan view of pixel regions;
Fig. 2 is a cross-sectional view along section line II-II of Fig. 1;
Fig. 3 shows a ray of light going through a gap between two pixel electrodes of Fig. 1;
Fig. 4 is a cross-sectional view along section line IV-IV of Fig. 1; and
Fig. 5 is a cross-sectional view along section line V-V of Fig. 1.

Fig. 1 shows an AMLCD substrate surface divided into pixel regions by the gate lines 34 and data lines 32 into pixel regions 100-102, 200-202 and 300-302. Each pixel region comprises a pixel electrode 38, a TFT 50, and a pixel electrode capacitor 74.

In Fig. 1, solid lines indicate the outlines of components that are on top and dotted lines indicate outlines of components that are underneath other structures. The pixel electrodes 38 are shown in solid lines because the pixel electrodes 38 is formed above the other components shown in Fig. 1.

The pixel electrode capacitor 74 is shown mostly underneath the pixel electrode 38, however, in the gap between two adjacent pixel electrodes 38, the perimeter of the pixel electrode capacitor 74 is above all other structures shown in Fig. 1 and thus is shown using solid lines.

The TFTs 50 is shown having source electrode 41, drain electrode 40 and etch stopper 60. The TFT 50 is below the pixel electrode 38. In the gap between the pixel electrodes 38, the outlines of the source electrode 41, the drain electrode 40 and the etch stopper 60 are the top structures and shown using solid lines. Although the source electrode 41 and the drain electrode 40 is formed over the etch stopper 60, the source electrode 41 and the drain electrode 40 do not cover the total surface of the etch stopper 60.

The data lines 32 are located vertically and are underneath the pixel electrodes 38. The outline of the data lines 32 are shown as vertical dotted lines. The source electrodes 41 are shown as extensions of the data lines 32. In the gap between the pixel electrodes 38, both the source electrodes 41 and the data lines 32 are above other components shown in Fig. 1 and thus are shown using solid lines.

The gate lines 34 are located horizontally and are underneath the data lines 32, the pixel electrode capacitors 74, the TFTs 50 and the pixel electrodes 38. Thus, the gate lines 34 are indicated by horizontal dotted lines. However, since the gate lines 34 is underneath all the other components, Fig. 1 only shows a few horizontal dotted lines between the other components.

Fig. 2 shows a cross-section along II-II of the pixel region 201, the TFT 50 corresponding to pixel 201 and the TFT 50 corresponding to pixel 101. The gate lines 34 are formed over the substrate 52. A gate insulating layer 56 is formed over the substrate 52 and the gate lines 34. Amorphous silicon layers 58 are formed over segments of the gate lines 34 on the surface of the gate insulating layer 56. The segments of the gate lines serve as gate electrodes for the TFTs 50. There are no additional structures extending from the gate lines 34 along their lengths to form the gate electrodes.

Etch stoppers 60 as shown in Figs. 1 and 2 are formed over each segment of the gate lines 34 which serves as gate electrodes. n+ layers 62 are formed over the amorphous layers 58 and parts of the etch stoppers 60. Metal layers 66 are placed over the n+ layers 62. The metal layers 66 and n+ layers 62 form the source electrode 40 and drain electrode 41 of each TFT 50. Thus, each TFT 50 comprises the source electrode 40, the drain electrode 41, the etch stopper 60, the amorphous silicon 58 and a portion of the gate insulating layer 56 that is formed over the segment of the gate line 34 that serves as a gate electrode.

A passivation layer 70 is formed over the TFTs 50 and the gate insulating layer 56. The passivation layer 70 is etched to expose the drain electrodes 41 and an ITO layer is formed over the passivation layer 70 and the drain electrodes 41. The ITO layer is patterned and etched to form the pixel electrodes 72.

The pixel electrode 72 corresponding to pixel region 201 is separated from the adjacent pixel electrodes 72 corresponding to pixel regions 101 and 301. The gap 712 between adjacent pixel electrodes 72 permits light to escape when the pixel 38 is dark for a normally clear liquid crystal material or when signals on the data or gate lines 32 or 34 changes the state of the normally opaque liquid crystal material. Thus the pixel electrode 72 is patterned so that the pixel electrode 72 extends over the gate line 34 by an overlap 710. Since the pixel electrode capacitor 74 holds the voltage potential of the pixel electrode 72 constant, the overlap 710 of the pixels electrode 72 over the opaque data and gate lines 32 and 34 functions as a dark matrix to block light escaping through the gaps between the pixel electrodes 72.

Fig. 3 shows a ray 704 of light escaping through the gap 712. The ray 704 forms a viewing angle 700 with a line perpendicular to the surface of the substrate 52. The magnitude of the viewing angle 700 is dependent on the relative values of the overlap 710 and the separating distance 718 between the bottom surface of the pixel electrode 72 and the top surface of the gate line 34. For this embodiment, the passivation layer 70 is about 6000 Å thick and the gate insulating layer 56 is about 3000 Å thick. Thus the separating distance 706 between the surface of the substrate 52 and the bottom surface of the pixel electrode 72 is about 9000 Å. Since the passivation layer 70 and the gate insulating layer 56 are formed over the gate line 34, the gate line thickness does not affect the thicknesses of the passivation layer 70 and the gate insulating layer 56. Thus, the separating distance 718 between the bottom of the pixel electrode 72 and the top surface of the gate line is also about 9000 Å.

To obtain a viewing angle of greater than 60 degrees, the overlap 710 must be at least about twice the separating distance 718. The tangent of the viewing angle is equal to the ratio of the separating distance 718 and the overlap 710. For a viewing angle of over 60 degrees, the ratio of the separating distance 718 and the overlap 710 must be greater than the tangent of 60 degrees. Since TAN 60 = v3 = 1.732, the ratio of the overlap 710 and the separating distance 718 must be greater than 1.732 or about 2. Thus, for a viewing angle of greater than 60 degrees, the overlap 710 should be about twice the separating distance 718. Accordingly, when the separating distance 718 is about 9000 Å, the overlap should be greater than 18000 Å to achieve a viewing angle of over 60 degrees.

The viewing angle is also affected by the accuracy

of the etching process. The photoresist pattern is shaped by a mask that is physically aligned with the structure already formed on the substrate 52. The combined masking and etching process is usually accurate to within about 1 μm. Thus, to guarantee a viewing angle of greater than 60 degrees, the overlap 710 must be at least 1 μm greater than 18000 Å. Since 1 μm is equal to 10,000 Å, to guarantee a viewing angle of greater than 60 degrees, the overlap 710 must be greater than 28000 Å or about 3 μm. Accordingly, the pixel electrode 72 must overlap the gate line 34 by about 3 μm to achieve a viewing angle of greater than 60 degrees.

Fig. 4 shows a cross-section of the data lines 32 along section line IV-IV. The amorphous silicon layer 58, the n+ layers 62 and the metal layers 66 form the data lines 32. The data lines 32 are formed above the surface of the gate insulating layer 56. Thus, to obtain a viewing angle of greater than 60 degrees, the overlap 708 between the pixel electrode 72 and the data line 32 should be about twice the separating distance 702 between the bottom surface of the pixel electrode 72 and the top surface of the data line 32.

The passivation layer 70 has a thickness of about 6000 Å. The passivation layer 70 is formed over the data line 32 and thus the data line 32 does not appreciably affect the separating distance 702 between the bottom surface of the pixel electrode 72 and the top surface of the data line 32. Accordingly, the separating distance 702 is about 6000 Å. To obtain a viewing angle of greater than 60 degrees, the overlap 708 must be greater than about 12000 Å. Accounting for the mask alignment accuracy of about 1 μm, the overlap must be greater than about 22,000 Å or about 2.1 μm to achieve a viewing angle of greater than 60 degrees.

Fig. 5 shows the structure of the intersection between the data line and the gate line along cross-section V-V. The gate lines 34 are formed over the substrate surface 52. The gate insulating layer 56 is formed over the substrate surface and the gate lines 34. The data lines 32 are formed over the gate insulating layer 56.

The etch stopper layer 60 is formed at the intersection between the amorphous silicon layer 58 and the n+ layer 62 of the data lines 32. This etch stopper layer 60 provides additional protection against shorts between the data lines 32 and the gate lines 34. Pin holes develop in the gate insulative layer 56 and the amorphous silicon layer 58. The n+ layer 62 and the metal layer 66 of the data lines 32 may form a contact to the gate lines 34 through the pin holes. The etch stopper layer 60 prevents this undesirable contact from forming.

The passivation layer 70 is formed over the gate insulating layer 56 and the data lines 32. The pixel electrodes 72 are formed over the passivation layer 70. The pixel electrodes 72 in Fig. 5 correspond to pixel 300 and pixel 201 and form a gap 716.

When the overlap 708 between the pixel electrode 72 and the data line 32 is greater than 2 μm, the viewing angle along the cross-section V-V will also be greater than 60 degrees. Since the separating distance 718 remains constant across the cross-section V-V while the overlap increases across a diagonal cut, the viewing angle increases along cross-section V-V.

The overlap of the pixel electrodes 72 over the gate lines 34 and data lines 32 introduces additional coupling capacitances between the pixel electrodes 72 and the gate and data lines 34 and 32, respectively. However, these parasitic capacitance values are small compared to the pixel electrode capacitor capacitance values. Thus, the noise effects caused by the additional parasitic capacitances are masked by the pixel electrode capacitors 74.

Since the dark matrix is obtained by overlapping the pixel electrodes 72 and the data lines 32 and gate lines 34, no new masks are introduced. The overlap is accomplished by the same masks that are used to form the gate and data lines 34 and 32, respectively, and the pixel electrodes 72.

However, the a-Si layer 58 of the TFT 50 forms the channel region of the TFT 50 and is very sensitive to light. When light enters the channel region of the TFT 50, the TFT 50 generates the leakage current which may cause the voltage potential of the pixel electrodes 72 to follow the data line voltages. For a normally opaque liquid crystal material, if sufficient light enters the TFT channel regions, the pixel electrodes 72 may become partially activated changing the state of the liquid crystal material. If this process continues, the pixel electrodes 72 activate erroneously. An opposite effect occurs for the normally clear liquid crystal material. The pixel becomes erroneously dark when the pixel electrodes 72 activate erroneously.

To guard against this potential problem, the dark matrix on the common electrode is retained to block light from affecting the TFT 50. Since the dark matrix no longer sets the aperture of the pixel, the dark matrix alignment requirements can be relaxed which simplifies the manufacturing process.

Moreover, instead of using the dark matrix to block light from the TFT 50, light filters can be used. For a color display, red, green and blue filters are used to cover the pixels. Light is sufficiently reduced by these filters to protect the TFTs 50. Since these filters can be formed to cover the TFT 50 without difficulty, processing steps required to form the dark matrix can be eliminated resulting in savings of at least one processing step.

Claims

1. An active matrix liquid crystal display device, comprising:

   a plurality of gate lines (34) formed over a substrate (52);

   a plurality of data lines (32) formed over the substrate; and

a plurality of pixel electrodes (38) formed over the substrate, wherein a perimeter of each of the pixel electrodes overlaps at least one of a portion of the gate lines and a portion of the data lines.

2. The active matrix liquid crystal display device of claim 1, wherein the pixel electrodes are a first distance (718) above the gate lines and a second distance (702) above the data lines, the perimeter of each of the pixel electrodes having at least one of a first portion (710) overlapping the portion of the gate lines by at least twice the first distance and a second portion (708) overlapping the portion of the data lines by at least twice the second distance to obtain a viewing angle of at least 60 degrees.

3. The active matrix liquid crystal display device of claim 2, wherein a separating distance (718) between a bottom surface of the pixel electrodes and a top surface of the gate lines is about 9000 Å and the pixel electrodes overlap (710) the gate lines by about 3 µm; and wherein a separating distance (702) between a bottom surface of the pixel electrodes and a top surface of the data lines is about 6000 Å and the pixel electrodes overlap (708) the data lines by about 2.1 µm.

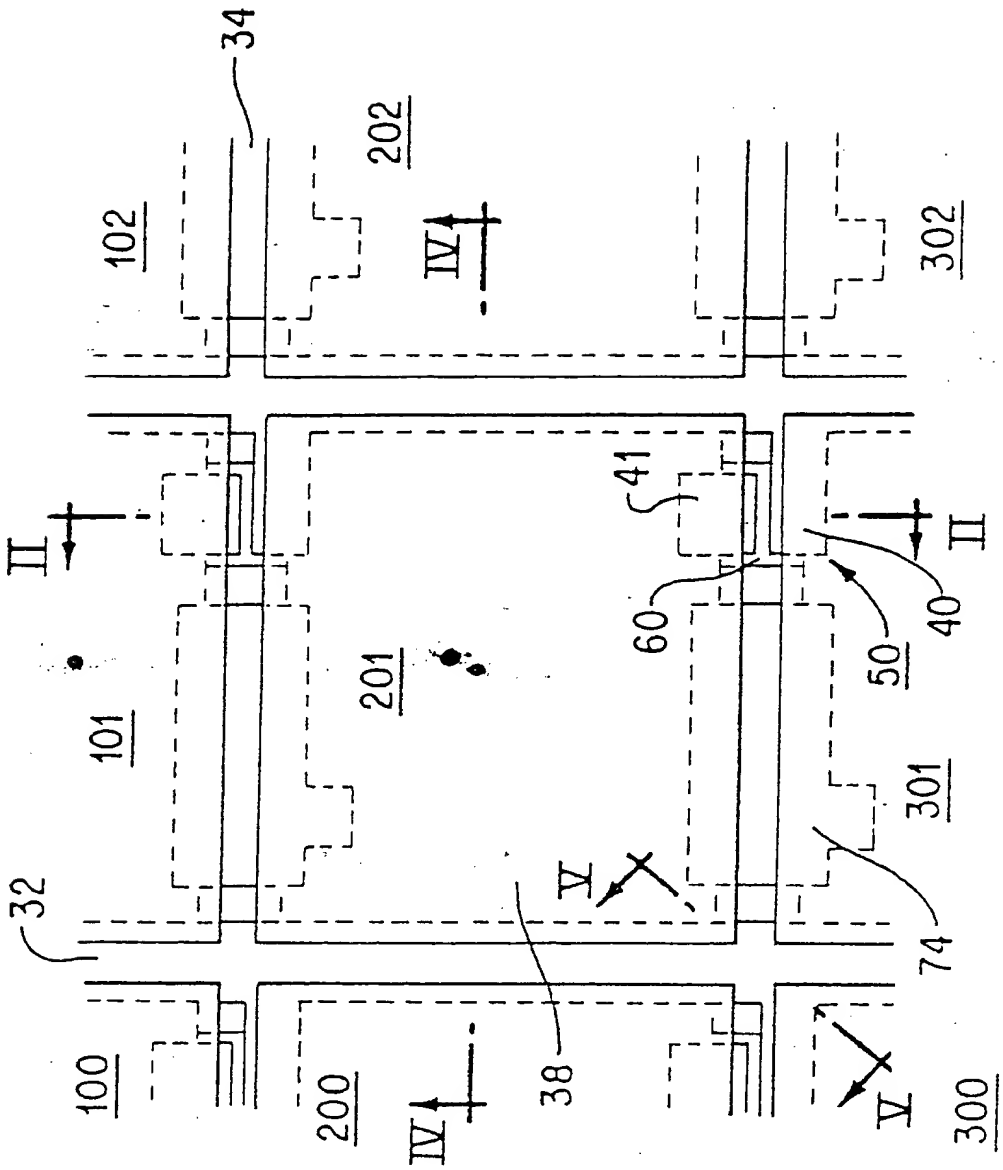
4. The active matrix liquid crystal display device of any one of claims 1 to 3, further comprising: a plurality of transistors (50) formed over the gate lines (34), wherein each of the gate lines has a plurality of segments and each of the plurality of segments of each gate line is a gate electrode of one of the plurality of transistors.

5. A method for manufacturing a dark matrix for an active matrix liquid crystal display device, comprising:

forming a plurality of gate lines (34) over a substrate (52);
forming a plurality of data lines (32) over the substrate;
forming a plurality of pixel electrodes (38) over the substrate; and
overlapping (708,710) a perimeter of each of the pixel electrodes over at least one of a portion of the gate lines and a portion of the data lines.

6. The method of claim 5, wherein the plurality of pixel electrodes are a first distance (718) above the gate lines and a second distance (702) above the data lines, a first portion of the perimeter of the pixel electrodes overlapping (710) the portion of the gate lines by at least twice the first distance and a second portion of the perimeter of the pixel electrodes overlapping (708) the portion of the data lines by at least twice the second distance to obtain a viewing angle of at least 60 degrees.

7. The method of claim 6, wherein a separating distance (718) between a bottom surface of the pixel electrodes and a top surface of the gate lines is about 9000 Å and the pixel electrodes overlap the gate lines by about 3 µm; and wherein a separating distance (702) between a bottom surface of the pixel electrodes and a top surface of the data lines is about 6000 Å and the pixel electrodes overlap the data lines by about 2.1 µm.


34
202
102
IV
302
II
41
II
60
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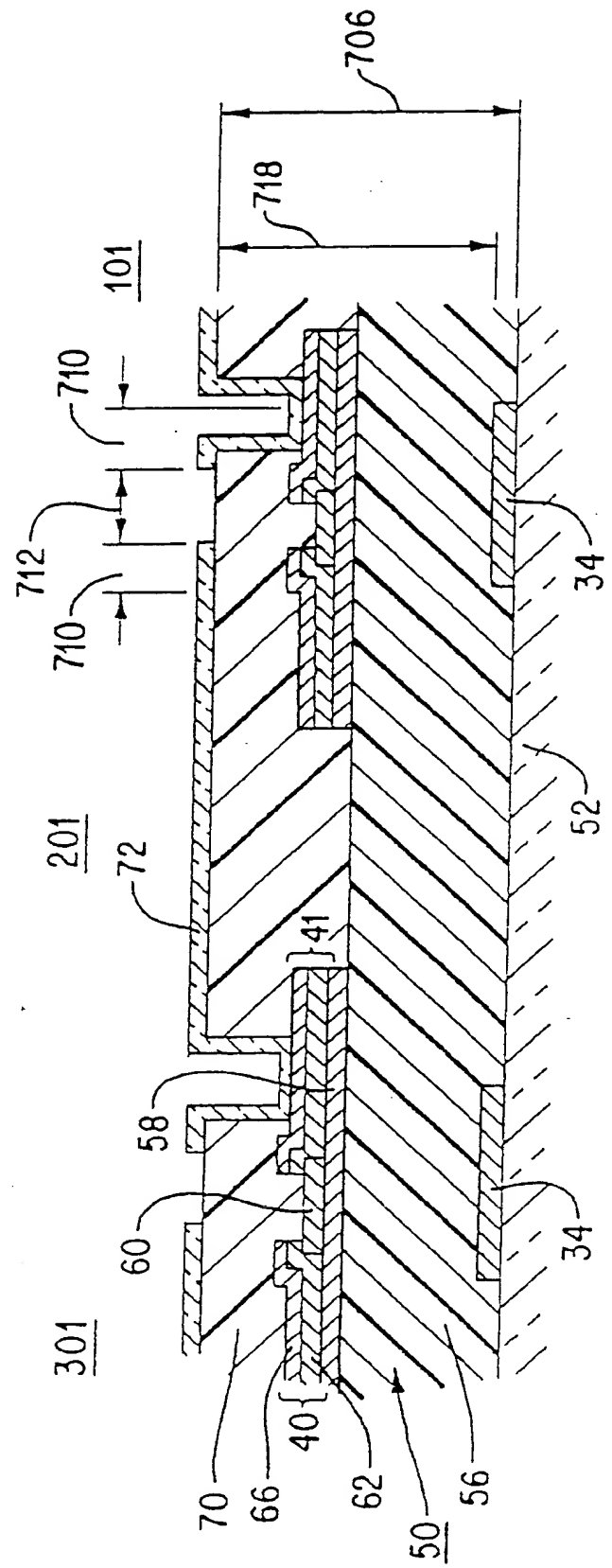
50
201
101
301
V
32
74
38
100
200
IV
V
300

FIG.1


706
718
101
710
712
710
34
52
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72
41
58
60
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301
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66
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62
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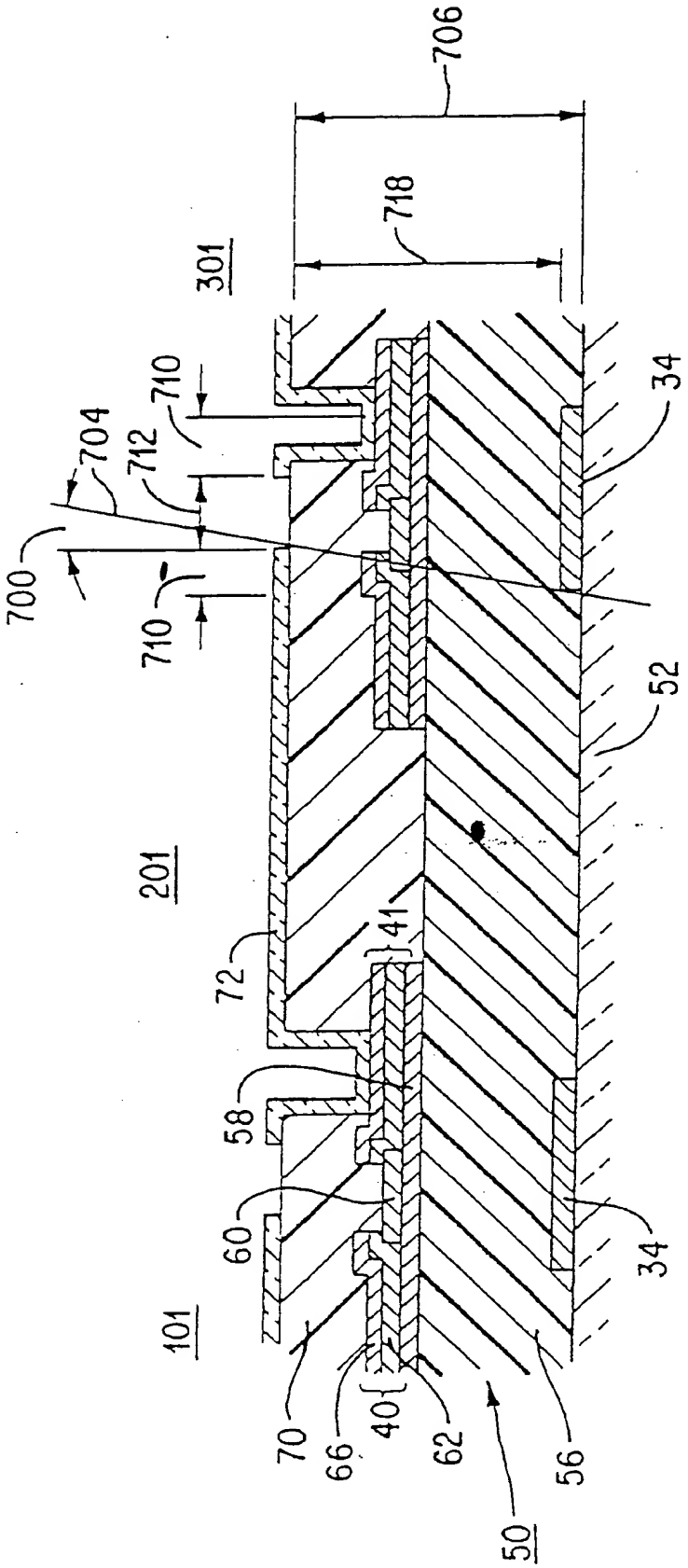
56

FIG. 2


706
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58
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FIG. 3

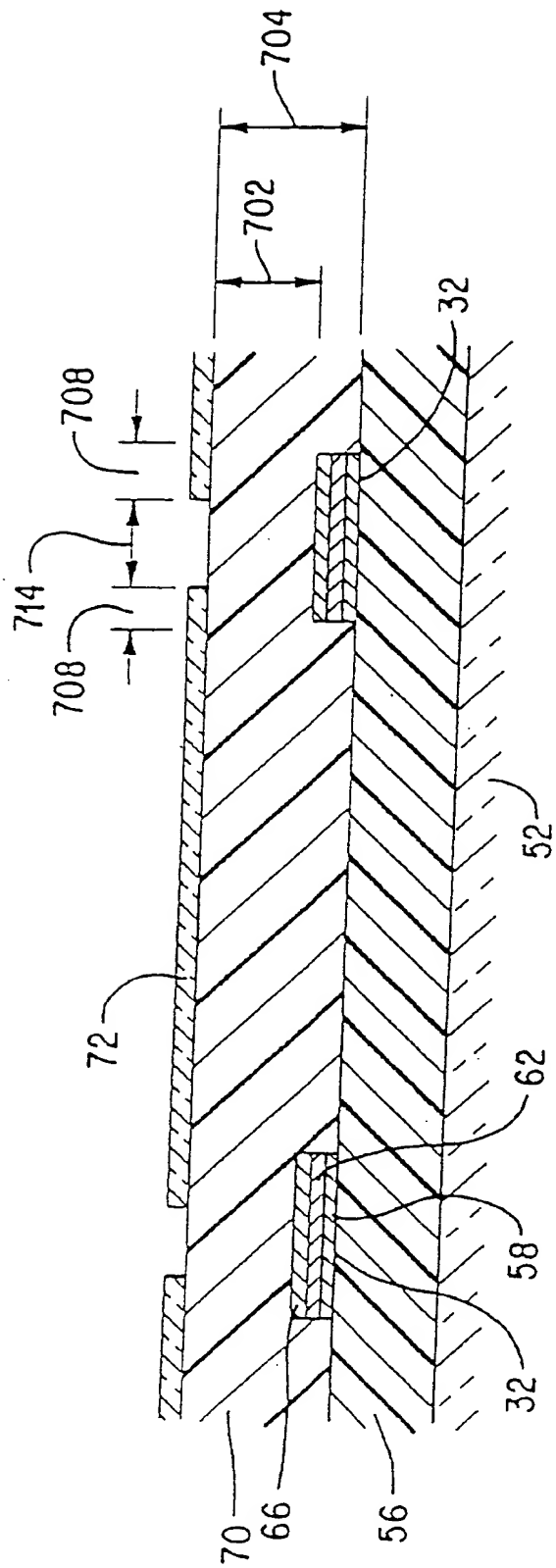

FIG. 4

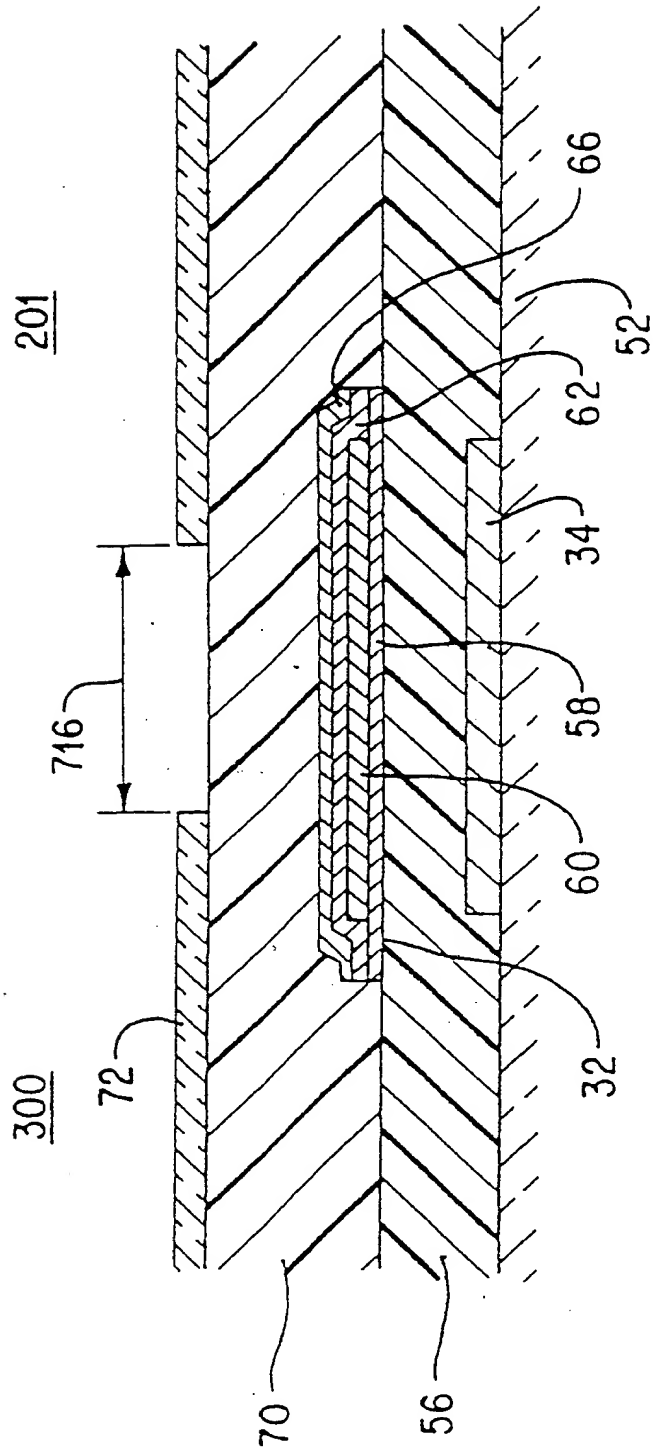

FIG. 5

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(71) Applicant: XEROX CORPORATION
Rochester, New York 14644 (US)

(72) Inventors:
- Yao, William
  Los Altos, California 94024 (US)
- Fulks, Ronald T.
  Mountain View, California 94049 (US)
- Ho, Jackson
  Palo Alto, California 94301 (US)

(74) Representative: Johnson, Reginald George et al
Rank Xerox Ltd
Patent Department
Parkway
Marlow Buckinghamshire SL7 1YL (GB)

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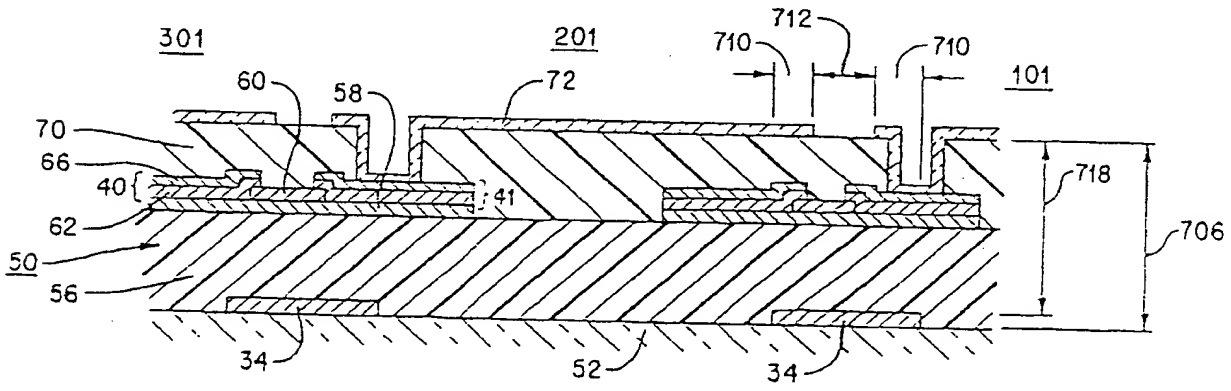

FIG. 2

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EUROPEAN SEARCH REPORT

Application Number
EP 96 30 3898

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	EP 0 603 866 A (SONY CORP) 29 June 1994 * column 19 - column 20; figures 12.14 *	1,5	G02F1/136 G02F1/1335
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 510 (P-1804), 26 September 1994 -& JP 06 175158 A (SEIKO EPSON CORP), 24 June 1994, * abstract *	1,4,5	
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 596 (P-1825), 14 November 1994 -& JP 06 222390 A (SANYO ELECTRIC CO LTD), 12 August 1994, * abstract *	1,5	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G02F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 March 1998	Wongel, H

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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EPO FORM 1503 03.82 (P04C01)

	Type	L #	Hits	Search Text	DBs	Time Stamp
21	BRS	L21	121	19 and ((data or signal) adj line with (black or shield$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 15:44
22	BRS	L22	1	"4568149".PN.	USPAT	2002/08/30 15:58
23	BRS	L23	1	"4938567".PN.	USPAT	2002/08/30 15:59
24	BRS	L24	1	"5327001".PN.	USPAT	2002/08/30 15:59
25	BRS	L25	1	"5426523".PN.	USPAT	2002/08/30 16:00
26	BRS	L26	1	"5682211".PN.	USPAT	2002/08/30 16:00
27	BRS	L27	1	"5686977".PN.	USPAT	2002/08/30 16:01
28	BRS	L28	1	"5696566".PN.	USPAT	2002/08/30 16:01
29	BRS	L29	1	"5708485".PN.	USPAT	2002/08/30 16:02
30	BRS	L30	1	"5767926".PN.	USPAT	2002/08/30 16:02
31	BRS	L31	1	"5877830".PN.	USPAT	2002/08/30 16:02
32	BRS	L32	1	"5708485".PN.	USPAT	2002/08/30 16:03
33	BRS	L33	1	"5696566".PN.	USPAT	2002/08/30 16:03
34	BRS	L34	1	"5459596".PN.	USPAT	2002/08/30 16:12
35	BRS	L35	1	"5822026".PN.	USPAT	2002/08/30 16:14
36	BRS	L36	1	"5847792".PN.	USPAT	2002/08/30 16:14
37	BRS	L37	1	"5953088".PN.	USPAT	2002/08/30 16:15

	Type	L #	Hits	Search Text	DBs	Time Stamp
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18	BRS	L18	0	17 and cut?off adj film	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 15:35
19	BRS	L19	916	349/110	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 15:41
20	BRS	L20	232	19 and ((data or signal) with (black or shield$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 15:44

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2	BRS	L2	1	"5151806".PN.	USPAT	2002/08/30 15:20
3	BRS	L3	1	"5182620".PN.	USPAT	2002/08/30 15:25
4	BRS	L4	1	"5345324".PN.	USPAT	2002/08/30 15:25
5	BRS	L5	1	"5345324".PN.	USPAT	2002/08/30 15:25
6	BRS	L6	1	"5394258".PN.	USPAT	2002/08/30 15:25
7	BRS	L7	1	"5426523".PN.	USPAT	2002/08/30 15:26
8	BRS	L8	1	"5446562".PN.	USPAT	2002/08/30 15:26
9	BRS	L9	1	"5453857".PN.	USPAT	2002/08/30 15:27
10	BRS	L10	1	"5453857".PN.	USPAT	2002/08/30 15:27
11	BRS	L11	1	"5459595".PN.	USPAT	2002/08/30 15:27
12	BRS	L12	1	"5528395".PN.	USPAT	2002/08/30 15:28
13	BRS	L13	1	"5151806".PN.	USPAT	2002/08/30 15:29
14	BRS	L14	1	"4704559".PN.	USPAT	2002/08/30 15:29
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76	BRS	L76	305	349/106.ccls. and tft	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 10:27
77	BRS	L77	157	76 and black adj matrix	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 10:28
78	BRS	L78	8	77 and (rubbing near alignment)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 10:29

	Type	L #	Hits	Search Text	DBs	Time Stamp
72	BRS	L72	0	1 and color adj overlap$4 adj (data or signal)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 09:47
73	BRS	L73	1	1 and color near (data or signal)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 09:49
74	BRS	L74	115	1 and color adj filter	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 09:49
75	BRS	L75	19	1 and (color adj filter with (data or signal))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 10:22

	Type	L #	Hits	Search Text	DBs	Time Stamp
50	BRS	L50	1	"5486493".PN.	USPAT	2002/08/30 09:22
51	BRS	L51	1	"5500750".PN.	USPAT	2002/08/30 09:22
52	BRS	L52	1	"5528209".PN.	USPAT	2002/08/30 09:23
53	BRS	L53	1	"5559055".PN.	USPAT	2002/08/30 09:24
54	BRS	L54	1	"5576630".PN.	USPAT	2002/08/30 09:24
55	BRS	L55	1	"5585951".PN.	USPAT	2002/08/30 09:24
56	BRS	L56	1	"5591676".PN.	USPAT	2002/08/30 09:24
57	BRS	L57	1	"5600458".PN.	USPAT	2002/08/30 09:24
58	BRS	L58	1	"5641974".PN.	USPAT	2002/08/30 09:24
59	BRS	L59	1	"5675187".PN.	USPAT	2002/08/30 09:25
60	BRS	L60	1	"5682211".PN.	USPAT	2002/08/30 09:25
61	BRS	L61	1	"5721596".PN.	USPAT	2002/08/30 09:26
62	BRS	L62	1	"5724111".PN.	USPAT	2002/08/30 09:26
63	BRS	L63	1	"5780874".PN.	USPAT	2002/08/30 09:26
64	BRS	L64	1	"5821621".PN.	USPAT	2002/08/30 09:27
65	BRS	L65	1	"5844647".PN.	USPAT	2002/08/30 09:27
66	BRS	L66	1	"5847720".PN.	USPAT	2002/08/30 09:27
67	BRS	L67	1	"5847720".PN.	USPAT	2002/08/30 09:28
68	BRS	L68	1	"5920084".PN.	USPAT	2002/08/30 09:28
69	BRS	L69	1	"5994721".PN.	USPAT	2002/08/30 09:29
70	BRS	L70	1	"6038008".PN.	USPAT	2002/08/30 09:29
71	BRS	L71	1	"6100954".PN.	USPAT	2002/08/30 09:29

	Type	L #	Hits	Search Text	DBs	Time Stamp
25	BRS	L25	1	"5294820".PN.	USPAT	2002/08/30 09:15
26	BRS	L26	1	"5302987".PN.	USPAT	2002/08/30 09:15
27	BRS	L27	1	"5302987".PN.	USPAT	2002/08/30 09:16
28	BRS	L28	1	"5364547".PN.	USPAT	2002/08/30 09:16
29	BRS	L29	1	"5408345".PN.	USPAT	2002/08/30 09:16
30	BRS	L30	1	"5408345".PN.	USPAT	2002/08/30 09:16
31	BRS	L31	1	"5409777".PN.	USPAT	2002/08/30 09:17
32	BRS	L32	1	"5411629".PN.	USPAT	2002/08/30 09:17
33	BRS	L33	1	"5414278".PN.	USPAT	2002/08/30 09:17
34	BRS	L34	1	"5414547".PN.	USPAT	2002/08/30 09:17
35	BRS	L35	1	"5419991".PN.	USPAT	2002/08/30 09:17
36	BRS	L36	1	"5426523".PN.	USPAT	2002/08/30 09:18
37	BRS	L37	1	"5446562".PN.	USPAT	2002/08/30 09:18
38	BRS	L38	1	"5446562".PN.	USPAT	2002/08/30 09:19
39	BRS	L39	1	"5453857".PN.	USPAT	2002/08/30 09:19
40	BRS	L40	1	"5457553".PN.	USPAT	2002/08/30 09:20
41	BRS	L41	1	"5459596".PN.	USPAT	2002/08/30 09:20
42	BRS	L42	1	"5463230".PN.	USPAT	2002/08/30 09:20
43	BRS	L43	1	"5463484".PN.	USPAT	2002/08/30 09:21
44	BRS	L44	1	"5459596".PN.	USPAT	2002/08/30 09:21
45	BRS	L45	1	"5463230".PN.	USPAT	2002/08/30 09:21
46	BRS	L46	1	"5463484".PN.	USPAT	2002/08/30 09:21
47	BRS	L47	1	"5466535".PN.	USPAT	2002/08/30 09:21
48	BRS	L48	1	"5477359".PN.	USPAT	2002/08/30 09:22
49	BRS	L49	1	"5483366".PN.	USPAT	2002/08/30 09:22

	Type	L #	Hits	Search Text	DBs	Time Stamp
5	BRS	L5	2	6376270.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/30 09:08
6	BRS	L6	1	"4431272".PN.	USPAT	2002/08/30 09:11
7	BRS	L7	1	"4451525".PN.	USPAT	2002/08/30 09:11
8	BRS	L8	1	"4636038".PN.	USPAT	2002/08/30 09:11
9	BRS	L9	1	"4943838".PN.	USPAT	2002/08/30 09:11
10	BRS	L10	1	"4980002".PN.	USPAT	2002/08/30 09:12
11	BRS	L11	1	"5003356".PN.	USPAT	2002/08/30 09:12
12	BRS	L12	1	"5045905".PN.	USPAT	2002/08/30 09:13
13	BRS	L13	1	"5055899".PN.	USPAT	2002/08/30 09:13
14	BRS	L14	1	"5055899".PN.	USPAT	2002/08/30 09:14
15	BRS	L15	1	"5045905".PN.	USPAT	2002/08/30 09:14
16	BRS	L16	1	"5072262".PN.	USPAT	2002/08/30 09:14
17	BRS	L17	1	"5177588".PN.	USPAT	2002/08/30 09:14
18	BRS	L18	1	"5182620".PN.	USPAT	2002/08/30 09:14
19	BRS	L19	1	"5229644".PN.	USPAT	2002/08/30 09:14
20	BRS	L20	1	"5246782".PN.	USPAT	2002/08/30 09:15
21	BRS	L21	1	"5281546".PN.	USPAT	2002/08/30 09:15
22	BRS	L22	1	"5281546".PN.	USPAT	2002/08/30 09:15
23	BRS	L23	1	"5287208".PN.	USPAT	2002/08/30 09:15
24	BRS	L24	1	"5287208".PN.	USPAT	2002/08/30 09:15